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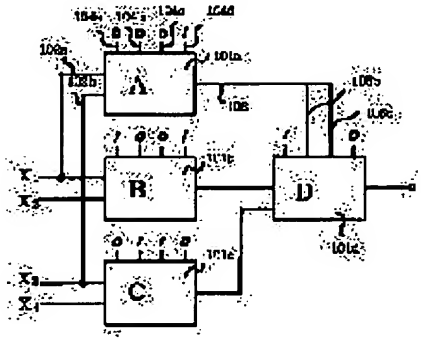
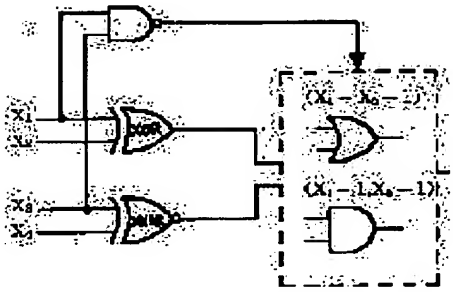
(54) ARITHMETIC UNIT

(57)Abstract:
PURPOSE: To enable flexible information processing similar to life body by inputting an output signal outputted from one of the output terminals or the result performing the prescribed arithmetic processing on the output signal to one of the 2nd input terminals.
CONSTITUTION: Respective arithmetic units A-D are provided with two input terminals 102a, 102b or the like, one output terminal 3, and four control signal input terminals 104a, 104b, 104c, and 104d or the like. Respective blocks A, B, C are made a NAND circuit and XOR circuit, and XNOR circuit by the input signals to the control input terminals 104a-104d. As two control input terminals 105b and 105c are not the constant signal but the output 103 of the block A is inputted as it is, the block D becomes an OR circuit if the output 103 is '0' and it becomes an AND circuit if it is '1'. A part corresponding to the block D is designed to have functions dissimilar by the NAND arithmetic result of X1 and X3.





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CLAIMS

[Claim(s)]
[Claim 1] Have two or more 1st input terminals and two or more 2nd input terminals, and predetermined data processing specified by the control signal inputted into said 2nd input terminal to the data signal inputted into said 1st input terminal is performed. In the arithmetic unit which has two or more arithmetic units which have at least one output terminal which outputs the result The arithmetic unit with which the result of having carried out predetermined data processing to the output signal or this output signal outputted from one of said the output terminals is characterized by being inputted into at least one of said the 2nd input terminal.
[Claim 2] Said arithmetic unit is an arithmetic unit according to claim 1 characterized by including the inverter which consisted of at least one step of neurone MOS transistors.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the arithmetic unit which enables flexible information processing especially with respect to an information processing technique.
[0002]
[Background of the Invention] These are called hardware although CPU of the core of the computer which performs an information processing technique consists of semi-conductors LSI conventionally. It is because that structure will be eternal and it will be an unchangeable strong thing, once it makes this reason. Having achieved the function with various computers is making the circuit where the function was fixed by the program perform work in good order. however, such now, although it must be what can respond also to information processing which the life object of study, adaptation, or self-multiplication which human being is performing itself is performing in order to realize future advanced information processing -- computer existence is not recognized.
[0003] On the other hand, although the attempt in which software skill will realize flexible information processing is also performed briskly, the actual condition is being unable to do very much well. Even if it realizes in false, paying [of software] becomes excessive, the reason is because hardware which is inflexible from the first is used as the base, even if it carries out with a supercomputer, great time amount is required, and the system which answers very much in an instant cannot be built.
[0004] Although research and development in the so-called neural network who imitated the cerebral information processing itself is done as one leading approach of solving this, this is also in a condition still far from utilization. The reason is in the situation which the essence of cerebral information processing hardly understands, very primitive structure is only imitated and the construction approach of concrete logic etc. is in a nil condition.
[0005] On the other hand, a highly efficient transistor called a neurone MOS transistor (artificer: Shibata direct, Tadahiro Omi, JP,3-6679,A) was invented, and the software hardware circuitry (artificer: Shibata direct, Tadahiro Omi:Japanese Patent Application No. No. 83135 [three to]) adapting this was invented. Especially this software hardware circuitry is a circuit which has the very flexible hardware which can change that calculation function freely with an external signal. Although the flexible information processing stated to the beginning might be realizable when using such flexible hardware as the base, the approach was not clarified until now.
[0006]
[Problem(s) to be Solved by the Invention] Then, this invention aims at offering the new arithmetic unit which enables indispensable study, adaptation, and flexible information processing of the life object of self-multiplication, and resemblance to future advanced information processing implementation.
[0007]
[Means for Solving the Problem] The arithmetic unit of this invention has two or more 1st input terminals and two or more 2nd input terminals. Predetermined data processing specified by the control signal inputted into said 2nd input terminal to the data signal inputted into said 1st input terminal is performed. In the arithmetic unit which has two or more arithmetic units which have at least one output terminal which outputs the result
[0008] to which the result of having carried out predetermined data processing to the output signal or this output signal outputted from one of said the output terminals is characterized by being inputted into at least one of said the 2nd input terminal

[Example] The example of this invention is explained using a drawing below.
[0009] (Example 1) Drawing 1 (a) is a block flow diagram which shows the 1st example of this invention. This circuit performs the next data processing to four digital input signals of X1-X4. X1=X3=1, if it becomes, it will be the arithmetic unit with which 1 is outputted at the time of X2=0 or X4=1, it is X1 !=X2 and 1 is outputted only at the time of X3=X4 when other (i.e., when either X1 or X3 are not equal to 1).
[0010] This circuit is made when even wiring connects mutually the logic unit of A, B, C, and four D (101a-101d). Each arithmetic unit has two input terminals (102a, 102b, etc.), one output terminal 103, and four control signal input terminals (104a, 104b, 104c, 104d, etc.), and the calculation function is prescribed by the signal of 0 or 1 inputted into a control input terminal. It means that 0 applies supply voltage VDD (5V) for 0V, and one applies an input terminal, respectively. The software hardware logic circuit (Japanese Patent Application No. No. 83135 [three to]) which used for example, the neurone MOS transistor (JP,3-6679,A) should just be used for such a circuit. A neurone MOS transistor and a software hardware logic circuit are explained separately.
[0011] Becoming a NAND circuit, an XOR circuit, and an XNOR circuit, respectively with the input signal to the control input terminal (104a-104d) shown in drawing only requires each block of A, B, and C. In Block D, since not a fixed signal but the output of Block A (NAND circuit) is inputted as it is, the two control input terminals 105b and 105c will serve as an AND circuit, if the output 103 becomes zero and it will be an OR circuit and 1. Drawing 1 (b) showed this relation intelligibly.
[0012] It is constituted so that the part equivalent to Block D may have the function which changed with results of the NAND operation of X1 and X3.
[0013] As shown above, when a circuit changes the function of a circuit of a part of the own one and changes the whole function by the result of an operation, the flexible calculation function is realized by this example.
[0014] Since the case of being very easy was illustrated above, the importance of a flexible new function is not necessarily in **, but after using and explaining drawing 2 -7 to a neurone MOS transistor list about a software hardware logic circuit about this, respectively, it explains in full detail in the 2nd example.
[0015] The structure and the principle of operation of a neurone MOS transistor (it abbreviates to nuMOS below) are explained first. Drawing 2 shows an example of the cross-section structure of the N channel nu MOS transistor of 4 inputs. 201 For example, the silicon substrate of P type, the source with which 202 and 203 were formed by N+ diffusion layer, and a drain, The gate dielectric film with which 204 was prepared on the channel field 205 between source drains (for example, SiO2 film), The insulator layer of for example, SiO2 grade and 208a, 208b, 208c, and 208d of the floating-gate electrode which 206 is electrically insulated and is in the condition of floating in potential, and 207 are control gate electrodes. Drawing 2 (b) is the drawing simplified further, in order to analyze nuMOS actuation. If the capacity-coupling multiplier between C1, C2, C3, C4, the floating gate, and a silicon substrate is set to C0 for the capacity-coupling multiplier between each control gate electrode and the floating gate as shown in drawing, potential phiF of the floating gate will be given by the degree type.
[0016]
phiF= (1-/CTOT) (C1V1+C2V2+C3V3+C4V4) (1)
However, CTOT=C0+C1+C2+C3+C4 (2)
the electrical potential difference on which V1, V2, V3, and V4 are impressed to the input gates 208a, 208b, 208c, and 208d, respectively -- it is -- the potential of a silicon substrate -- 0V -- that is, it was presupposed that it is grounded.
[0017] Now, potential of the source 202 is set to 0V. That is, it considers as the value which measured the potential of all electrodes on the basis of the source. Then, if nuMOS shown in drawing 2 is the same as the usual N-channel metal oxide semiconductor transistor if it considers that the floating gate 206 is the usual gate electrode, and the gate potential phiF becomes size from a threshold (VTH*), between source drains will be connected electrically. Namely, (1) type (CTOT) (C1V1+C2V2+C3V3+C4V4) > VTH* (3)
When ****** is filled, nuMOS is that [flow (it turns on)].
[0018] Although the above is explanation about an N-channel metal oxide semiconductor transistor, the device which drawing 2 (a) Set and used altogether the source 202, the drain 203, and the substrate 201 as the reverse conductivity type also exists. That is, a substrate is N type, is nuMOS in which the source drain was formed by P+ diffusion layer, and calls this a P channel MOS transistor.
[0019] A neurone circuit, a soft hardware logic circuit next the most fundamental circuit using nuMOS, a

neurone circuit, and its actuation are explained using drawing 3 . The neurone circuit is made from nu MOS inverter 212 and the usual inverter 213 which consisted of N channel nuMOS210 and P channel nuMOS211. This circuit is a circuit where nu MOS inverter is reversed in when potential phiF of the common floating gate 214 exceeds the turn over voltage (1/2) VDD of nu MOS inverter, and VOUT becomes 1. In drawing, it of CTOT and **** gate set all (1/8) the capacity-coupling multipliers of the V1 - V4 gate to CTOT (1/2), and since it was easy, it assumed them to be Co=0. **** gate is called the main electrodes of nu MOS inverter.

[0020] Actuation of this circuit is easily analyzable with floating-gate potential drawing (Floating-Gate Potential Diagram = FPD and abbreviated name) shown in drawing 4 . FPD is what expressed phiF as a function of ****, and if it becomes V1-V4=0, when **** changes from 0 to VDD, phiF will change from 0 (1/2) to VDD. That is because the joint capacity of **** is CTOT (1/2). That is, the output of a neurone circuit is always 0.

[0021] In the example of drawing 4 , by V1=V2=0 and V4=VDD, **** is VDD to0-(3/4) VDD, and, as for V3, the case where it is set to 0 is illustrated at ****>(3/4) VDD. If it carries out like this, in phiF, VOUT will output 1 by ****>(1/2) VDD. What is necessary is just to input **** into V3, after a threshold lets the pre inverter 214 of VDD (3/4) pass as shown in drawing 5 if you think that he will realize such a circuit. The same circuits have been the bases of a software hardware logic circuit (Soft Hardware Logic circuit = SHL and abbreviated name).

[0022] Next, an example of a SHL circuit is explained using drawing 6 and 7. The circuit diagram was shown in drawing 6 . 301 is the D/A converter formed in the input stage, and generates the multiple-value variable **** of 4 level to the combination of two inputs X1 and X2. **** is inputted into the main gates of five nu MOS inverters 302-306. The relation between X1, X2, and **** is shown in the axis of abscissa of FPD of drawing 7 (a). Va, Vb, Vc, and Vd support the control signal input terminals 104a-104d of the operation block A of drawing 1 . The capacity-coupling multiplier between each input gate and the floating gate has shown the fraction of 1/2, 1/4, and a 1 / 8 grades in drawing, and it means CTOT, CTOT (1/4), CTOT (1/8), etc., respectively (1/2).

[0023] In this circuit, the binary signal of Va, Vb, Vc, Vd0, or VDD is inputted. Drawing 7 (a) showed FPD of nu MOS inverter 302 about the case of Va=Vb=Vc=Vd=1 (= VDD). An output is set to 0 to the combination of all inputs. An example of FPD to the combination of others of Va, Vb, Vc, and Vd and an output was shown in drawing 7 (a), (b), (c), and (d). It turns out that the reversal signal of the signal inputted into Va, Vb, Vc, and Vd is outputted corresponding to = (X2, X1) (0 0), (0, 1), (1, 0), and (1, 1). Since an output pattern can be specified by direct Va-Vd and a function form can be decided, it is the big description that a function can be determined easily.

[0024] The circuit of drawing 6 is an example of SHL to the last, and it cannot be overemphasized that SHL of others which are indicated by the patent specification (Japanese Patent Application No. No. 83135 [three to]) may be used.

[0025] (Example 2) The 2nd example of this invention is shown in drawing 8 below. This considers one nu MOS inverter as an operation block, is the arithmetic circuit which consisted of eight blocks, and serves as the number adder of binary SD. When performing an add operation conventionally and bit length became long in order to progress to count of the upper bit, after performing addition from a low-ranking bit most and calculating beam raising (carry) each time, in proportion to it, the delay of the operation time was large. It had become a serious failure at the time of this performing high-speed data processing.

[0026] This example realizes an adder without the so-called carry propagation whose beam raising affects only the next beam immediately, and will not be able to realize it without by changing a part of functions of a circuit block easily using a part of result of an operation using a SHL circuit. The number system of SD is first explained before this example.

[0027] One of the number systems expressing the signal of a multiple value is the number system [1] of Signed-Digit(SD). Although the number system of SD is a style with redundancy, so, the outstanding description is in it as ****. For example, in addition and subtraction of the number of SD, regardless of the word length, propagation of a carry is limited only to one step, and an operation advances to juxtaposition mostly. If this description is employed efficiently, a high-speed operation will be attained.

[0028] The number of binary SD is several X defined as follows.

X=an-1 2n-1+an-2 2n-2 + ... +a1 2+a0ai ** (-1, and {0, 1})

That is, although a single figure (1 bit) is the number system which takes the value of three values, it is not the number of ternaries but a binary number. That is, it is a redundant number system. For example, with the number of binary SD, (1, -1, and 0) show the same number as (0, 1, 0). Such addition of the number of SD is considered. xi, yi, and its linearity addition sum are set to zi for i figures of the two numbers of binary SD.
[0029] xi ** (-1, and {0, 1})
yi ** (-1, and {0, 1})
zi =xi+yi ** (-2, -1, and {0, 1, 2})
They are zi =2ci+wici and wi ** (-1, and {0, 1}) to this zi.
What is necessary is just to ask for a carry and the medium sum on the conditions shown in a table 1 in consideration of linearity addition sum zi-1 of a lower bit at this time, although it asks for Carry ci and the medium sum wi to satisfy.
[0030]
[A table 1] The carry c of SD adder, and table of truth value of the medium sum w

z i	z i-1	c i	w i
2	*	1	0
1	≧0 <0	1 0	−1 1
0	*	0	0
−1	<0 ≧0	−1 0	1 −1
−2	*	−1	0

If linearity addition of carry ci-1 from the medium sum wi which was able to be found here, and a lower bit is carried out, the final sum si will be called for. Since the carry is generated in consideration of the linearity addition sum of a lower bit at the time of the above-mentioned conditional judgment, a carry carry does not occur by the operation which asks for the final sum. Therefore, propagation of a carry is limited only between ******** bits. The above is the algorithm of the number addition of SD.
[0031] In order to realize this algorithm by nuMOS, the number of binary SD of three values was first coded in binary number of 2 bits. When nu MOS inverter is used for this, the output of an inverter is because it becomes binary. A coding table is shown in a table 2 and a table 3.
[0032]
[A table 2] Coding of the number of binary SD, and a 2-bit binary number

2進SD	2進数	
1 0 −1	1 0 0	1 1 0

[0033]

z	x+y
2	1が4個
1	1が3個
0	1が2個
−1	1が1個
−2	1が0個

[A table 3] Coding of the linearity addition sum w

When making the number of SD of three values into the binary number of 2 bits, it coded paying attention to the number of 1. About z which is the linearity addition sum of x and y, it coded in the number of 1 contained in x and y. According to this coding, the table of truth value of the above-mentioned SD addition is rewritten. Moreover, zi-1 which is the linearity addition sum of a low order digit divides table of truth value into two by 0 or more and less than 0. The rewritten table of truth value is shown in a table 4.

[0034]

[A table 4] Table of truth value rewritten for nuMOS logical circuits

（a）制御信号が1の時（$z_{i-1} \geqq 0$） （b）制御信号が0の時（$z_{i-1} < 0$）

z i	c i		w i	
1が4個	1	1	0	1
1が3個	1	1	0	0
1が2個	0	1	0	1
1が1個	0	1	0	0
1が0個	0	0	0	1

z i	c i		w i	
1が4個	1	1	0	1
1が3個	0	1	1	1
1が2個	0	1	0	1
1が1個	0	0	1	1
1が0個	0	0	0	1

Here, if a control signal is 1 or less than 0 with [linearity addition sum zi-1 of a lower bit] zero [or more], it is a variable which takes 0. The column of a high order bit and the right shows [the column of the left divided by the dotted line about ci and wi all over the truth table] a lower bit.

[0035] What realized table of truth value shown with a table 4 using nuMOS logical circuit is shown to drawing 9 by the circuit diagram. This is a circuit which takes out and draws the circuit blocks 401-404 of drawing 8 , and outputs the reversal signal of Carry Ci and each sum Wi to Xi and Yi.

[0036] The symmetric-function nuMOS logical circuit of 2-bit a total of 4-bit input of 2 bits and y of Input x is used. The number of 1 which is the result of coding z turns into the main variables **** of nu MOS inverter as it is. What drew the number of one in Z for FPD of nu MOS inverters 401-404 as a main variable **** is shown in drawing 10 , and 11, 12 and 13, respectively.

[0037] For example, when a control signal CTRL is 0 and 00001 and a control function are 1 as a target function (property of an output), what is necessary will be just to set up 00011 in nu MOS inverter (drawing 10) which calculates the high order bit of Carry c. That is, the input terminal 405 of a control signal CTRL is committing the control signal input terminal which determines the calculation function of the operation blocks 401 and 402. The terminal 406 into which Xi and Yi are inputted is a data signal input terminal. It is the function form in CTRL=1 which the dotted line and the hatch way (407 c-f) showed by drawing 10 -13, and it is the function form in CTRL=0 which the continuous line (408 c-f) showed.

[0038] Thus, the number adder (SDFA) circuit of SD of drawing 9 is realized. Carry c and the medium sum w are outputted with the reversal (negation) value for simplification of a circuit. nu MOS inverter which calculates the high order bit of the above-mentioned carry is the leftmost inverter 401. Here, nu MOS inverter 403 which

calculates the high order bit of the medium sum w is considered. As for this neurone circuit, a target function is set to 01010 when a control signal is 0. This is an XOR function. However, a target function is set to 00000 when a control signal is 1. Thus, in order to calculate the high order bit of the medium sum w, this nu MOS inverter arithmetic unit calculates an XOR function with a control signal CTRL, or is not concerned with an input but is changing that function as it is as outputting 0 ****. Here, the output of nu MOS inverters 401 and 402 which calculate a carry was inputted into the control signal input terminal 409 which opts for the function of arithmetic units 403 and 404, and has changed the function if needed. This has realized the operation of the medium sum.

[0039] Drawing 14 shows all the single figure adding the number of binary SD of a circuit. The control signal CTRL is made by one nu MOS inverter (410) and the control circuit which usually consisted of one inverter (411). Moreover, s which it is as a result of [final] addition is obtained by performing addition of the carry from the medium sum w and a low order digit with the linearity adder (414) which consisted of two nu MOS inverters (412 413).

[0040] As mentioned above, the adder of the number of binary SD has constituted very easily by this invention. In addition, the transistor count needed was only 16 per figure, and it was completely impossible to have realized in an easy circuit in this way until now.

[0041] The number adder of binary SD described above is a circuit which outputs and inputs the signal which coded the number of binary SD in binary number of 2 bits. However, if it is the number of binary SD expressed with the forward electrical-potential-difference value, it is possible to combine with the floating gate of nu MOS inverter directly with 3 value signals. Moreover, an output can also be outputted after changing the binary output of 2 bits into the number of SD of three values in nuMOS source follower circuit. That is, SD adder stated by this example is the circuit which can interface easily, and the binary signal and the signal of a multiple value are extremely rich in versatility.

[0042] (Example 3) The 3rd example of this invention is shown in drawing 15 R> 5. Here, the example of representation is shown using arithmetic unit A which generally has n input terminals 501 for data signals. The output of Unit A is stored in a flip-flop 502, and the output is applied to some control input terminals 503 which specify the own function of unit A again. The shift register controlled by the clock is sufficient as this flip-flop. In this way, when predetermined delay is put into the output of A and it puts into a control input terminal, the function will change based on the past result of an operation. That is, a self output will be fed back and it will opt for a function.

[0043] A still more extensive calculation function can be given by adding such memory functions.

[0044] The output of a memory device or a delay element 502 may be inputted into the control input terminal 505 of a different unit B from A (504) like drawing 16 .

[0045] (Example 4) Drawing 6 is the 4th example of this invention, and the output of A is inputted into the binary counter 506. It is the example which applied the triplet to which the count set to 1 was counted, and A was binary and coded the count to the decision of a function. It cannot be overemphasized that you may use for the functional decision of other natural blocks also in this case.

[0046] Since the structure can be changed or the circuit itself can make a new function based on its result of an operation according to this invention above, the study which becomes indispensable in a highly informative society, adaptation, and flexible information processing similar to the life object of self-multiplication are realizable. And the computer by which an algorithm and architecture completely differ from the former can be realized now.

[0047] As mentioned above, although the floating gate of nu MOS inverter described ******** only when always using it in the state of floating, this may attach the switch transistor 701 to the floating gate like drawing 18 , and may connect it with the predetermined potential Vm. Or the value of this potential may be used as other data. Moreover, it cannot be overemphasized that actuation of omitting the penetration current which the signal Vs which has controlled the switch is synchronized with a system clock, and returns the charge in the floating gate to an initial state each time, or flows to an inverter may be carried out.

[0048]

[Effect of the Invention] By this invention, it becomes realizable [the new processing unit which enables study, adaptation, and flexible information processing of the life object of self-multiplication, and resemblance], and advanced information processing is attained.

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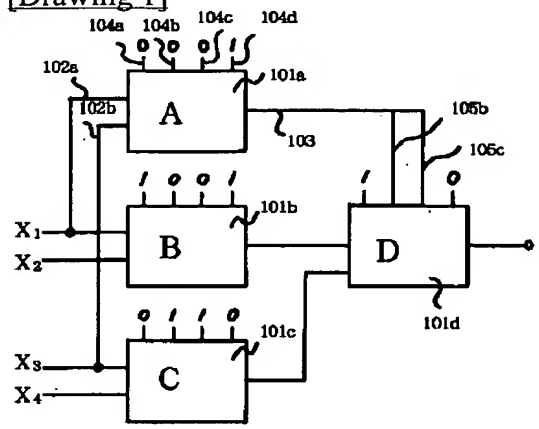
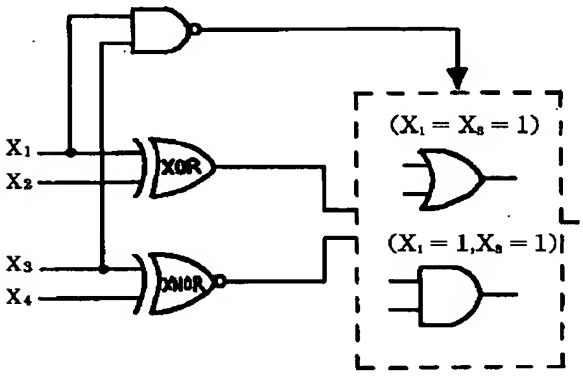
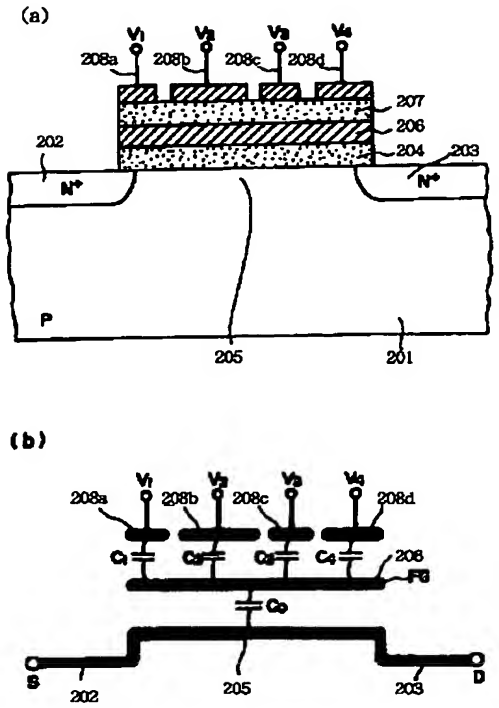
DRAWINGS

[Drawing 1]

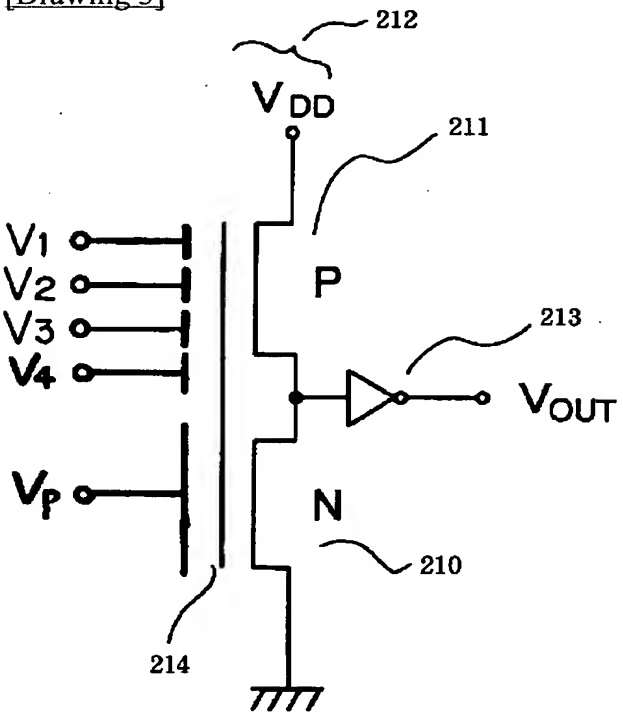




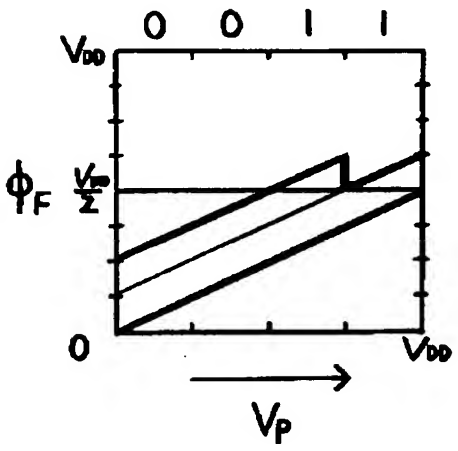
[Drawing 2]



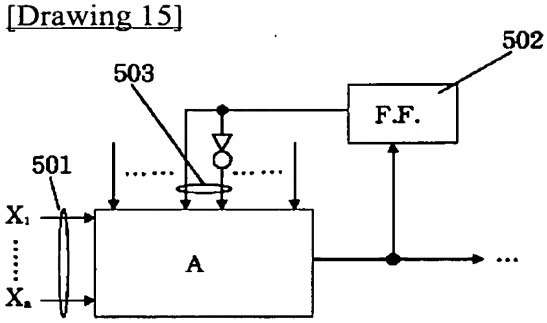
[Drawing 3]



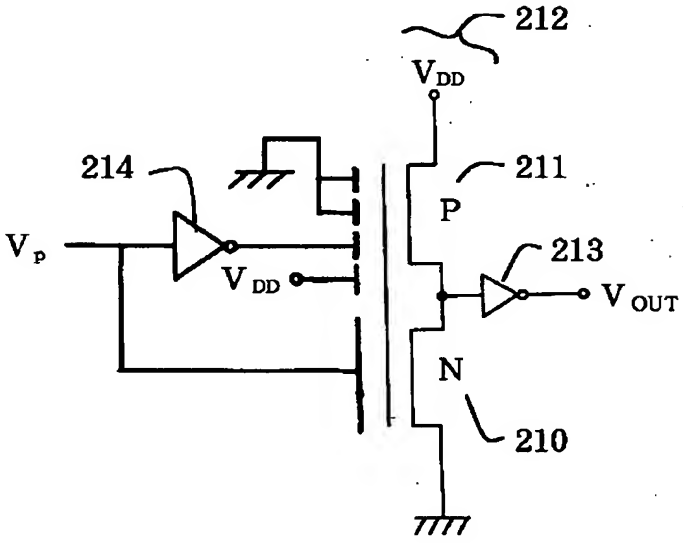
[Drawing 4]



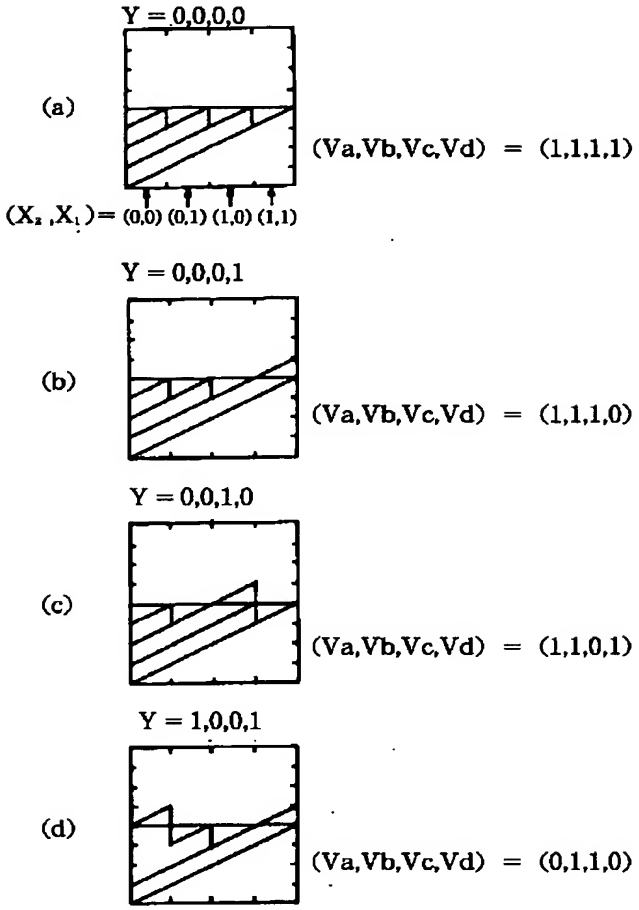
[Drawing 15]



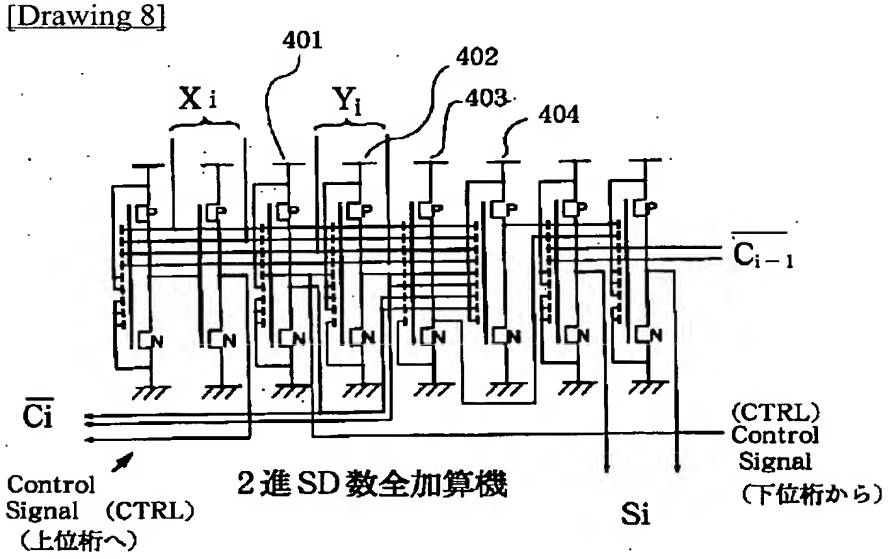
[Drawing 5]



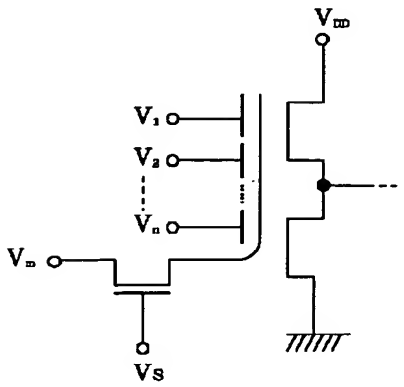
[Drawing 7]



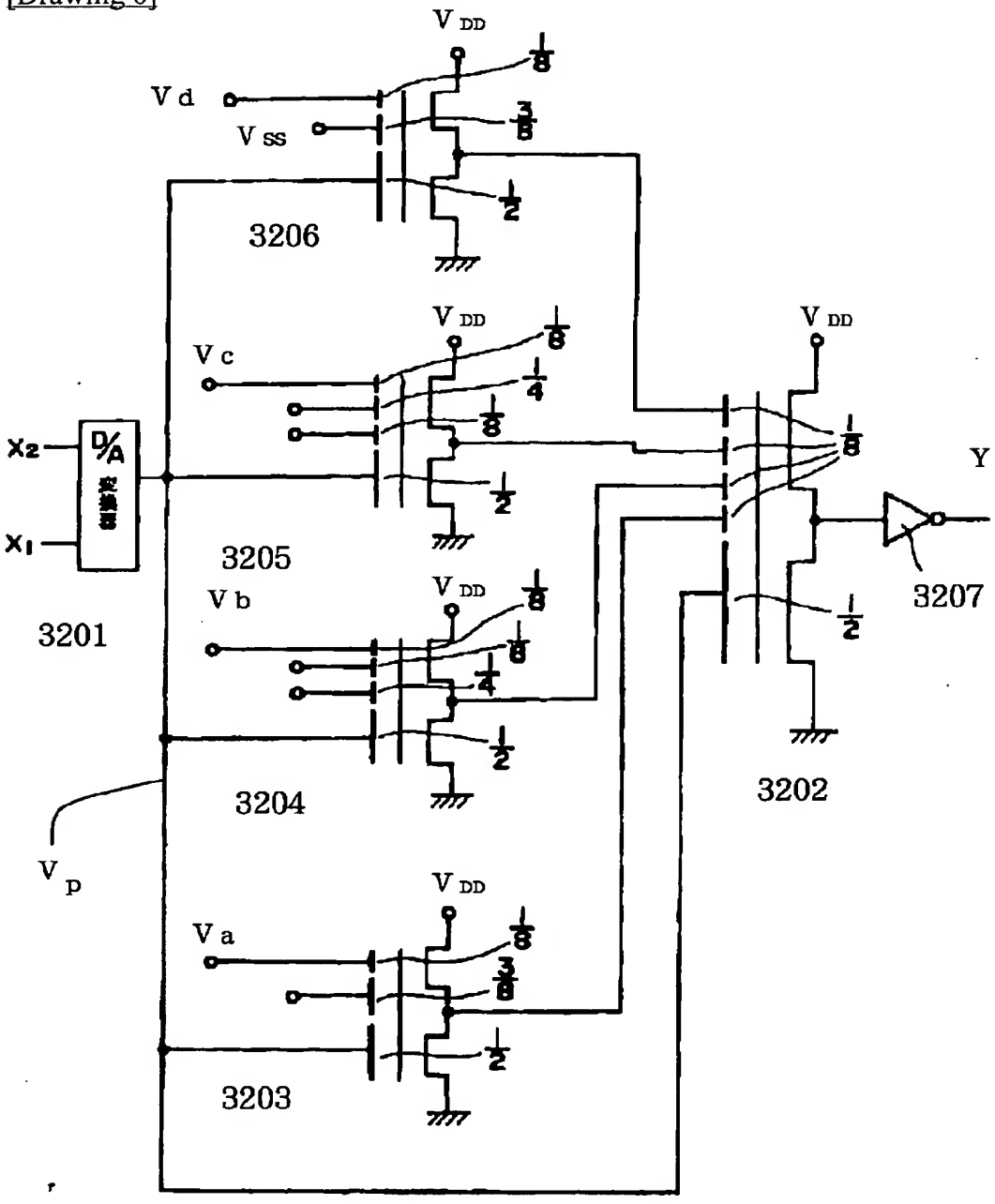
[Drawing 8]



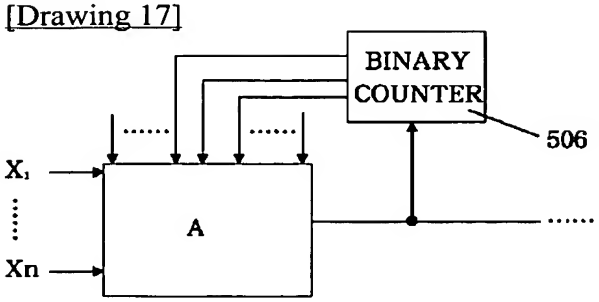
[Drawing 18]


V_{DD}
V_1
V_2
V_n
V_m
Vs

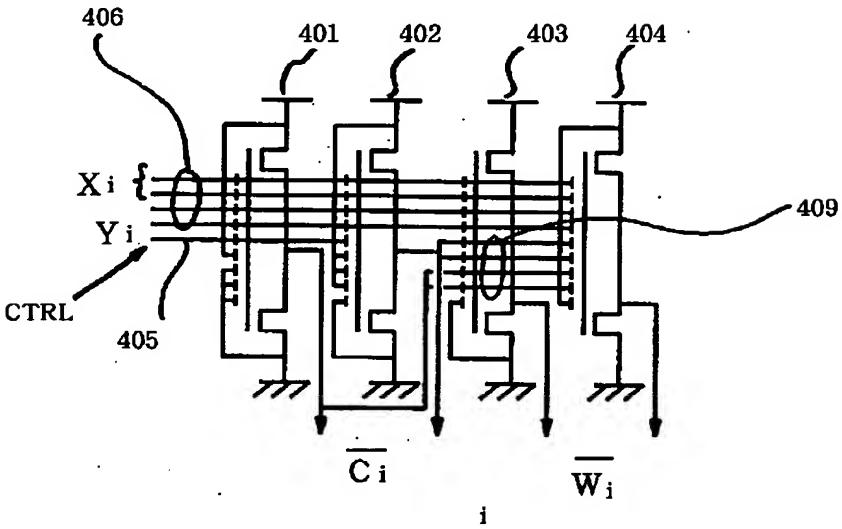
[Drawing 6]


V DD
Vd
V ss
3206
V DD
Vc
V DD
X2
D/A
X1
3201
3205
Vb
V DD
3204
Vp
V DD
Va
3203
V DD
Y
3207
3202

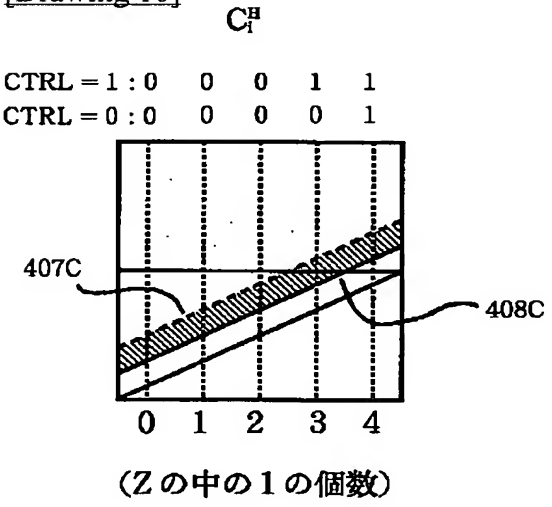
[Drawing 17]



[Drawing 9]

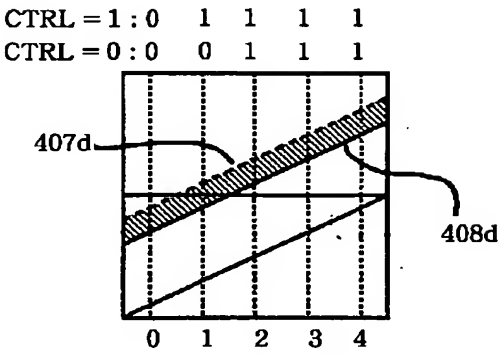


[Drawing 10]



[Drawing 11]

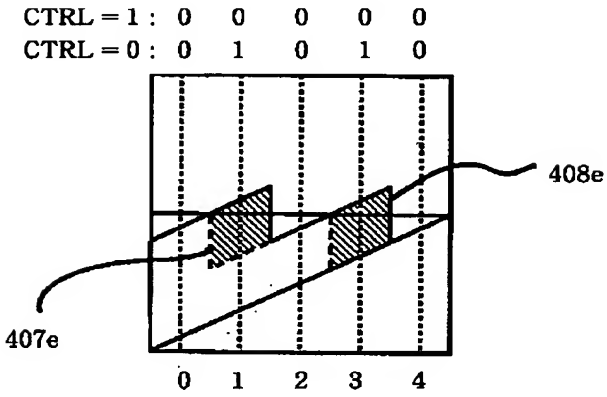
C_i^L



(Zの中の1の個数)

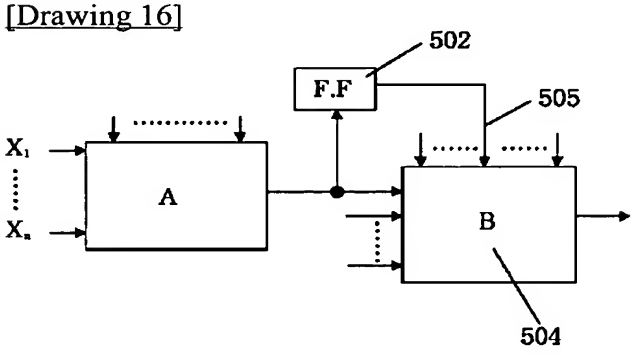
[Drawing 12]

W_i^n

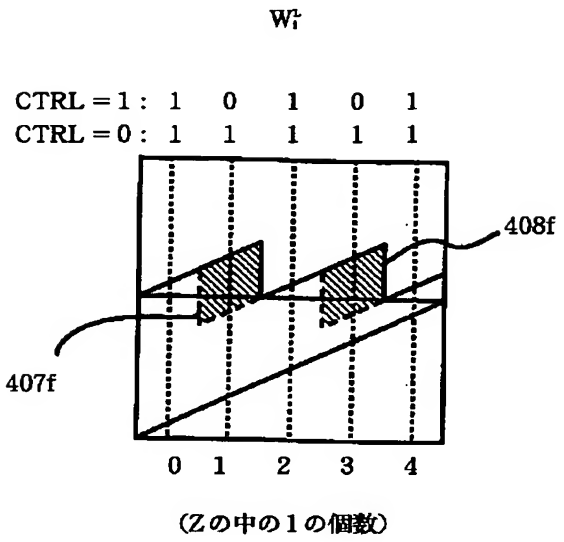


(Zの中の1の個数)

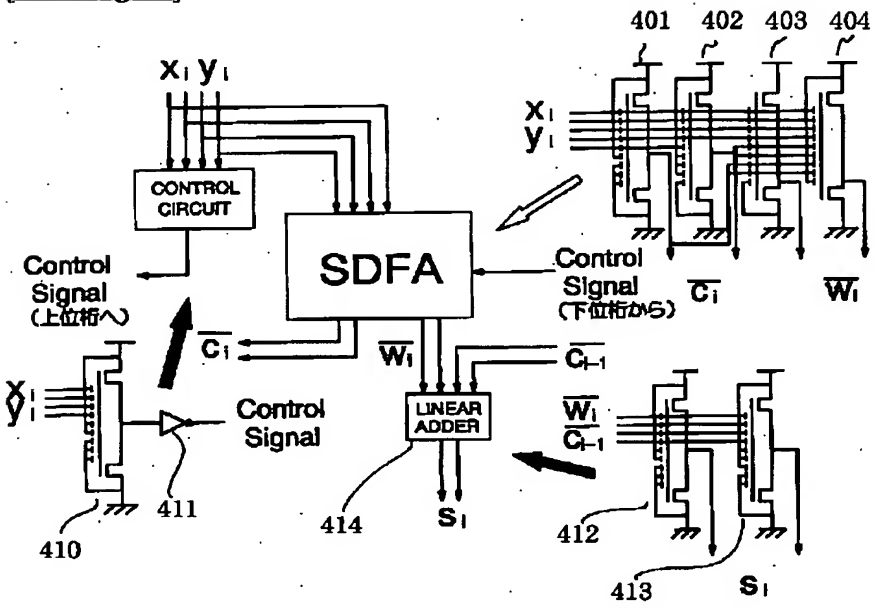
[Drawing 16]



[Drawing 13]



[Drawing 14]



[Translation done.]